

IRFR/U120N

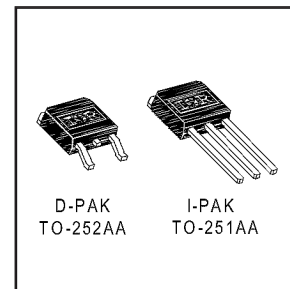
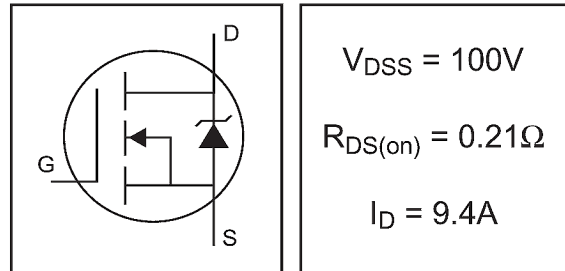
HEXFET® Power MOSFET

- Surface Mount (IRFR120N)
- Straight Lead (IRFU120N)
- Advanced Process Technology
- Fast Switching
- Fully Avalanche Rated

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The D-PAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.



Absolute Maximum Ratings

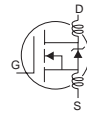
	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	9.4	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	6.6	
I_{DM}	Pulsed Drain Current ①⑥	38	
$P_D @ T_C = 25^\circ C$	Power Dissipation	48	W
	Linear Derating Factor	0.32	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②⑥	91	mJ
I_{AR}	Avalanche Current①⑥	5.7	A
E_{AR}	Repetitive Avalanche Energy①⑥	4.8	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	3.1	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount) **	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS/ΔT_J}	Breakdown Voltage Temp. Coefficient	—	0.12	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.21		V _{GS} = 10V, I _D = 5.6A ④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
g _{fs}	Forward Transconductance	2.7	—	—	S	V _{DS} = 25V, I _D = 5.7A⑥
I _{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V _{DS} = 100V, V _{GS} = 0V
		—	—	250		V _{DS} = 80V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V
Q _g	Total Gate Charge	—	—	25	nC	I _D = 5.7A
Q _{gs}	Gate-to-Source Charge	—	—	4.8		V _{DS} = 80V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	11		V _{GS} = 10V, See Fig. 6 and 13 ④⑥
t _{d(on)}	Turn-On Delay Time	—	4.5	—		ns
t _r	Rise Time	—	23	—	I _D = 5.7A	
t _{d(off)}	Turn-Off Delay Time	—	32	—	R _G = 22Ω	
t _f	Fall Time	—	23	—	R _D = 8.6Ω, See Fig. 10 ④⑥	
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact⑤
L _S	Internal Source Inductance	—	7.5	—		
C _{iss}	Input Capacitance	—	330	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	92	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	54	—		f = 1.0MHz, See Fig. 5⑥



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	9.4	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①⑥	—	—	38		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 5.5A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	99	150	ns	T _J = 25°C, I _F = 5.7A
Q _{rr}	Reverse Recovery Charge	—	390	580	nC	di/dt = 100A/μs ④⑥
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② V_{DD} = 25V, starting T_J = 25°C, L = 4.7mH R_G = 25Ω, I_{AS} = 5.7A. (See Figure 12)
- ③ I_{SD} ≤ 5.7A, di/dt ≤ 240A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 175°C
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%
- ⑤ This is applied for I-PAK, L_s of D-PAK is measured between lead and center of die contact
- ⑥ Uses IRF520N data and test conditions

** When mounted on 1" square PCB (FR-4 or G-10 Material) .
For recommended footprint and soldering techniques refer to application note #AN-994

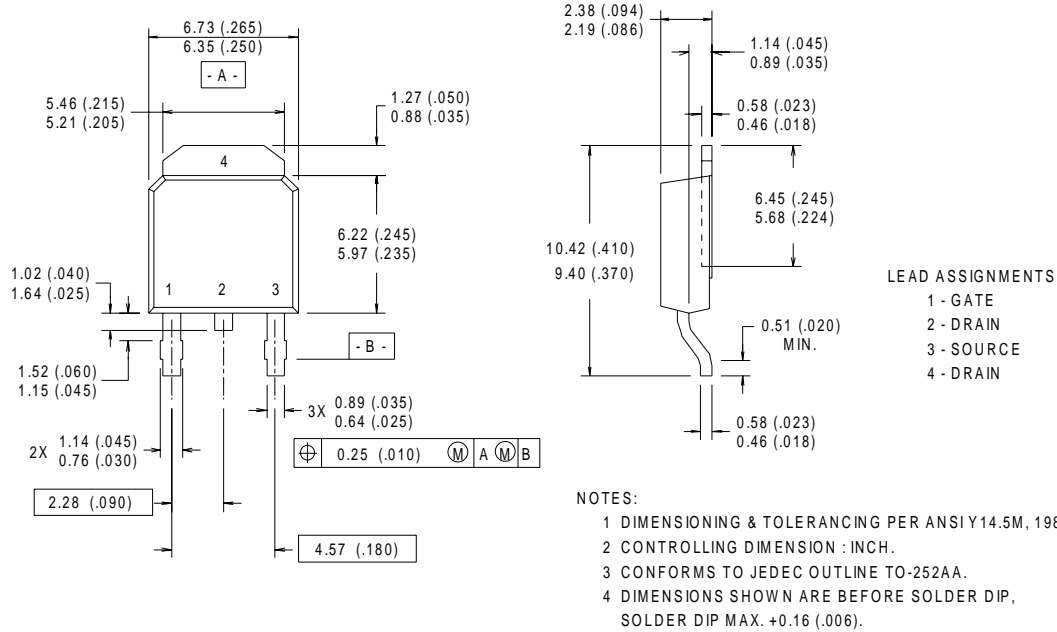
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Package Outline

TO-252AA Outline

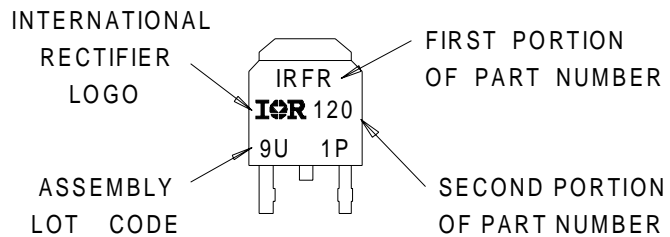
Dimensions are shown in millimeters (inches)



Part Marking Information

TO-252AA (D-PARK)

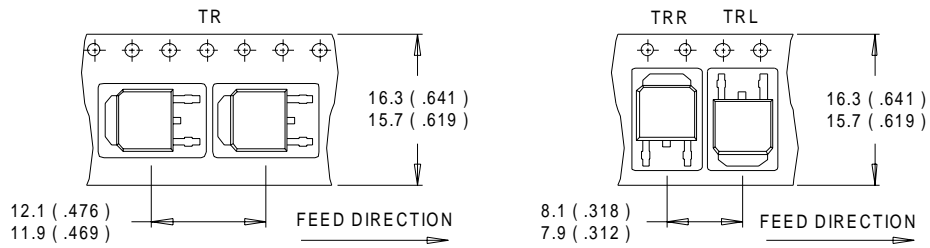
EXAMPLE : THIS IS AN IRFR120 WITH ASSEMBLY LOT CODE 9U1P



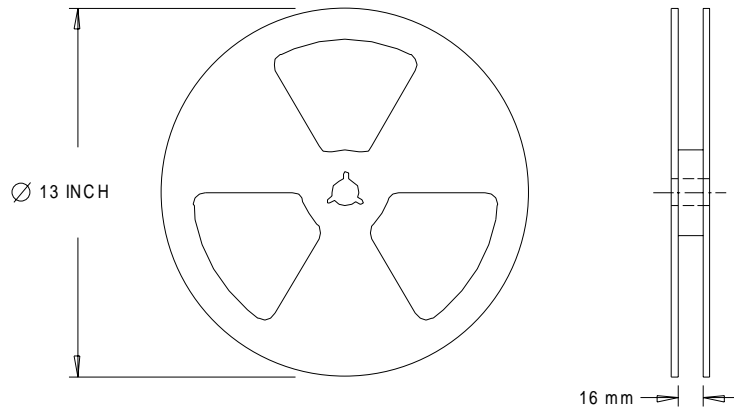
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Tape & Reel Information

TO-252AA



- NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES :
1. OUTLINE CONFORMS TO EIA-481.